is a non-recoverable parity error, generating an indication of the non-recoverable interrupt error and storing the indication in the processor's registers.

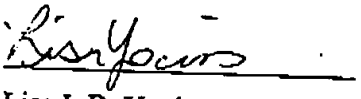
The Examiner rejected claims 24 and 29 under 35 U.S.C. § 103(a) as being unpatentable over *Quach* in view of U.S. Patent 6,445,717 issued to *Gibson*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Claim 29 has been canceled. Claim 24 describes the communications unit being one of a modem and Ethernet adapter in combination with a processing unit that is connected to the bus system, where the processing unit includes registers for storing a single set of processor information that indicates an error type, error states, and error status to form stored processor information in response to the detection of a parity error in the cache that is associated with the processor and determining whether the parity error is a recoverable parity error using the stored processor information by reading said registers to analyze said stored error type, error states, and error status. The combination of *Quach* and *Gibson* does not describe, teach, or suggest the combination of these features.

Applicants' claims are believed to be patentably distinct over the prior art because the prior art does not describe, teach, or suggest Applicants' claims. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 06.29.04

Respectfully submitted,



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